User Standard Case Build Usage

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**Abstract:**

TMP core script will be created to support all cases in LSH with the same case format. This case description will cover general introduction and details for FPGA case format.

REVISION HISTORY

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# 1 Objective

TMP Core Script Spec—Case Building focus on the general core script work flow and the detail work flow on case building, including the case structure, detail requirements and default setting for every folder or file and the demo cases.

# 2 TMP Core Script Work Flow(FPGA)

Script will run a design case step by step: get design entry, run implement flow, run simulation flow and finally run check and report flow.

Here is a top level flow chart for script work flow.



Figure1. Script work flow

## 2.1 Design entry

Script will scan the test case to find the design entry. With the different information in test case, script will pass down into different implement work flow. Here are the scan rules for making a decision.

1. Scan case folder for a file with name like xx.info
2. Scan xx.info file for LDF file information.

Here is a flow chart for script running in this process:



Figure2. Entry work flow

\*NOTE:

1. TCL work flow:

Test case have a project file (which also can be rebuild from RTL/EDF files), script will run like Diamond GUI flow (open project, run implement, run simulation…).

1. CMD work flow:

Test case doesn’t have project file, script will run in command line flow (use input files to run foundry commands defined in “cmd\_flow” section, such as: map, par).

## 2.2 Implement flow

Implement flow will run the test case according the flow steps defined by info file or external options. Since we have two different design entries, so implement will be a little different from each other.

### 2.2.1 Implement flow for TCL flow

TCL flow will support the following option:

1. Device-kit: user can change project device info
2. No-scuba: user can disable update scuba command line in project files
3. Strategy update: user can update strategy setting
4. Run process: user can specific a run process (run map, run par, run par trce … )
5. Sweeping: user can run sweeping flow
6. Multi-seed: user can run multi-seed flow

Here is a flow chart for TCL flow:



Figure3. TCL work flow

\*NOTE: Implement prepare: will be creating work path, design information collection.

### 2.2.2 Implement flow for CMD flow

CMD flow is for standalone command line support, with this flow support, user can run PAR command line with MAP NCD file and PRF file. CMD flow will support the following options and flow.

1. Run process: user can specific a run process (run map, run par, run par trce … )
2. Run process(engine) with specific command line
3. Sweeping: user can run sweeping flow(not support now)
4. Multi-seed: user can run multi-seed flow(not support now)

Here is a flow chart for CMD flow.



Figure4. CMD work flow

\*Currently we don’t support sweeping flow and multi-seed flow.

\*Sanity check uses the following rules:

1) User should list all the input files for the run command(s). For example: When a user want to run MAP command, the device information and NGD file were required in the info file, if there are one more flow specified by user, such as: PAR, one more LPF file should be list in the info file.

2) The default flow command line will be used while there is no specific command line find in info file.

3) User should list all run flows step by step, i.e. user input files are map ncd and prf files and user want to run par and par trace, user should list the following lines in “[cmd\_flow]”:

a) run\_par = 1

b) run\_trce = 1

\*for actually options please refer to BQS help document.

## 2.3 Simulation flow

Simulation flow is for those test cases need to run simulation. We can find the simulation information from the info file.

Currently simulation flow support simulation for all of the following styles with both ModelSim & Active-HDL.

1. RTL simulation flow
2. POST map simulation flow
3. POST par simulation flow

For every of these three flows, BQS script support:

1. Source file simulation flow
2. Macro(.do) file simulation flow

BQS script will treat these options as add on option, this means script will run what the script get form arguments:

1. Get run RTL simulation: RTL simulation will be run
2. Get run RTL & MAP simulation: RTL & MAP simulation will be run
3. Get run RTL & PAR simulation: RTL & PAR simulation will be run
4. Get run RTL, MAP & PAR simulation: RTL, MAP & PAR simulation will be run.

Here is a flow chart for simulation flow:



Figure5. Simulation flow

## 2.4 Check & report flow

Check report flow is used to check the test case implement status and report the implement info. We use “xx.conf” file to specify the check and report information for script use. And here is top level flow chart:



Figure6. Check & report flow

# 3 Case Building

## 3.1 Case Structure:

The general structure for a standard case will like the following:

--testdata/ data for data driven case test

--testdesign/ real test design

--testmethod/ test scripts or method

--bqs.conf result check file

--bqs.info run boot file (flow, simulation run)

--readme.txt case info

## 3.2 info file building

Info file will be dividing into four sections: project section, simulation section, flow section, command line section.

The following description are based on FPGA flow(Diamond, ICECube2)

### 3.2.1 Project Section

Project section used to record project information, this section should start with “[qa]” and use the following options:

1. ldf\_file= used to address the ldf file
2. Inc\_path= include extra path for rebuilding project file use
3. others\_path= address other path for rebuilding project use
4. base\_lpf= address original lpf file for rebuilding project file use
5. devkit= device information for rebuilding project file use
6. top\_module=<rtl\_top> specify the top module for rebuilding project file use
7. src\_files= list all source files for rebuilding project file use
8. edf\_file= edf files
9. map\_ngd= map NGD file for MAP CMD flow implement
10. map\_ncd= map NCD file for PAR CMD flow implement
11. lpf\_file= lpf file for PAR CMD flow implement
12. par\_ncd= par NCD file for TRCE CMD flow implement
13. par\_prf= par PRF file for TRCE CMD flow implement
14. project\_name= project name setting
15. impl\_name= implementation name setting
16. …

\*value list in “<>" are default values, if the value not given or these options not shown in project section will be considered as use the default values

We can simply divide these options into three classes:

1. LDF entry: use this ldf file for design entry.(a)
2. SRC entry: use these source files to rebuilding project file and entry LDF entry.(b-g)
3. CMD entry: use the given individual files for standalone command run.(h-p)

And the priority will be: LDF entry > SRC entry > CMD entry

### 3.2.2 Simulation Section

Simulation section used to record simulation information, this section should start with “[sim]” and with the following options:

1. dev\_lib=<> used to address which device lib should be used
2. pri\_lib=<work> used to address which lib should be used first
3. tb\_file= used to address the test bench file
4. tb\_vector=<test\_vector.in> used to address the simulation input vector
5. sim\_top=<sim\_top> used to address test bench top model name
6. uut\_name=<UUT> used to address instance name of top RTL module
7. sim\_time= <10 us> how long is the simulation will be run
8. do\_msim= ModleSIM simulation macro file
9. do\_ahdl= active-HDL simulation macro file
10. do\_qsim= questasim simulation macro file

\*value list in “<>" are default values, if the value not given or these options not shown in simulation section will be considered as use the default values

\*\*For “dev\_lib” please leave it blank there or just omit this option to make the script search the right device simulation library automatically (according current device and language style). If you write any device library here, script will use the specific device library and ignore the current project device and language style. So take care!

\*\*\*please always write the right simulation time for “sim\_time” which can be “<x> us” or “-all”. Please replace “<x>” to the right number you wanted.

We can simply divide these options into three classes:

1. LIB path: simulation libraries should be used.(a-b)
2. SRC entry: source files for simulation use.(c-f)
3. Macro entry: macro files for simulation use.(g)

LIB path should be always used for simulation. While different entry (b, c) will implement different simulation flow and the priority will be: b > c.

### 3.2.3 Flow Section

Flow section is for implement flow use, this section should start with “[cmd\_flow]”. Here is an example:

1. run\_scuba = 0
2. run\_synthesis = 1
3. synthesis = synplify
4. synp\_goal = Timing
5. run\_translate = 1
6. run\_map = 1
7. run\_map\_trce = 1
8. run\_par = 1
9. run\_par\_trce = 1

While a “1” means this flow should be run, “0” or omit means this flow should not be run.

### 3.2.4 Command Section

Command section is for CMD flow use, this section should start with “[command]”, it will replace the default implement command line with given command line.

The default command lines for implementation engine are:

Table : default command

|  |  |  |
| --- | --- | --- |
| NO. | CMD Name | Default CMD line |
| 1 | edif2ngd | edif2ngd -l "@(family)s" -d @(pty)s "@(edf\_file)s" "@(ngo\_file)s" |
| 2 | ngdbuild | ngdbuild -a "@(family)s" -d @(pty)s "@(ngo\_file)s" "@(ngd\_file)s" |
| 3 | map | map -a "@(family)s" -p @(pty)s -t @(pkg)s -s @(spd)s -oc @(opt)s "@(ngd\_file)s" -o "@(map\_ncd)s" -pr "@(prf\_file)s" -mp "@(mrp\_file)s" -lpf "@(lpf\_file)s" |
| 4 | map\_trce | trce -v 1 -gt -mapchkpnt 0 -sethld -o "@(tw1\_file)s" "@(map\_ncd)s" "@(prf\_file)s" |
| 5 | map\_vsim | ldbanno "@(map\_ncd)s" -n Verilog -o "@(map\_vo)s" -w -neg |
| 6 | map\_vhdsim | ldbanno "@(map\_ncd)s" -n VHDL -o "@(map\_vho)s" -w -neg |
| 7 | par | par -w -l 5 -i 6 -t 1 -c 0 -e 0 -exp parUseNBR=1:parCDP=auto:parCDR=1:parPathBased=OFF "@(map\_ncd)s" "@(par\_ncd)s" @(prf\_file)s |
| 8 | par\_trce | trce -v 10 -gt -sethld -sphld m -o @(twr\_file)s @(par\_ncd)s @(prf\_file)s |
| 9 | par\_iotiming | iotiming "@(par\_ncd)s" "@(prf\_file)s" |
| 10 | export\_vsim | ldbanno "@(par\_ncd)s" -n Verilog -o "@(par\_vo)s" -w -neg |
| 11 | export\_vhdsim | ldbanno "@(par\_ncd)s" -n VHDL -o "@(par\_vho)s" -w -neg |

If you want to change the default command line, just write your command line in this section, such as: par\_trce = trce -v 12 -gt -sethld -sphld m -o @(twr\_file)s @(par\_ncd)s @(prf\_file)s. here “@(xx)s” will be replaced when script run.

## 3.3 conf file building

We dividing conf file into three sections: configuration section, method section, check section. With these configurations script can run check and report, while there is no conf file find, script will also create a default conf file for implement flow check.

### 3.3.1 Configuration Section

This section is for report title configures:

1. area= configure the top model name
2. type= configure the sub model name
3. cr\_note= current test case fail reason CR or others
4. cr\_fixed= fixed CRs or problems

If area = STA, type= Features you will see the following information in the report file:

Table1. Report example

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Area | Type | Case | Device | Result | Comments |
| STA | Features | xxxx | xxxx | xxxx |  |

### 3.3.2 Method Section

This section is for check result generate. Here is an example:

1. check\_block\_1 = 1
2. check\_block\_2 = 0
3. check\_lines\_1 = 1
4. check\_data\_1 = 1

Let’s take item a as an example: “check\_block\_1” is a method name, “1” means check flow will check this method, in this condition there must be a “check\_block\_1” method to specify how to run check flow. If “check\_block\_1 = 0” mean check flow will not run check flow.

If all methods list in this section passed check, we fill find “PASS” in the report file for this case.

### 3.3.2 Check Section

Check section is used to define how to run check flow, currently we support the following check flows:

#### 3.3.2.1 check\_lines

1) format

[check\_lines]

title = check\_test1

file = <path>\<file>

check\_1 = <string\_1>

times = <number> --optional

check\_<num> = <string\_2>

2) description

This method will try to find the <string\_1> assigned by check\_1 in <file> and treat it as a start point (line 1),

(If times option is used, scripts will find <string\_1> <number> times and then treat the last one as start point),

Then try to check whether line <num> (a shift value) has <string\_2>. if yes, the result of this method is true.

#### 3.3.2.2 check\_data

1) Format

[check\_data]

file=<path>\<file>

start\_line = <string\_1>

times = <number> --optional

result = <num> / <line>,<shift>

line<num1> = <num>,<operation\_symbol> / <line>,<shift>,<operation\_symbol>

line<num2> = <num>,<operation\_symbol> / <line>,<shift>,<operation\_symbol>

...

line<numn> = <num> / <line>,<shift>

2) Description

this method will try to find the <string\_1> assigned by start\_line in <file> and treat it as a start point (line 1),

(if times option is used, scripts will find <string\_1> <number> times and then treat the last one as start point),

Then try to calculate the result.

User can either use the absolute number or to use the line + shift to indicate the number.

#### 3.3.2.3 check\_block

1) Format

[check\_block]

Title = check\_blocks

compare\_file = <path>\<file>

golden\_file = <Gold\_file>

2) Description

This method will try to compare the <Gold\_file> and <file>, if <Gold\_file> is included in <file>, return true.

#### 3.3.2.4 check\_flow

1) Format

[check\_flow]

file=<path>\<file>

2) Description

this method will try to find the string "All signals are completely routed." in the par report.

<file> need to be a par report.

#### 3.3.2.5 check\_multiline

1) Format

[check\_multiline]

file = <path>\<file>

check\_line = <total\_string>

2) Description

This method will try to find the <total\_string> assigned by check\_line in <file> regardless the "space" and "line feed".

This method will benefit the situation that the <total\_string> won't be at the same line and changing for each regression.

## 3.4 testdata folder building

This folder used for the collection of test data if have.

## 3.5 testmethod folder building

This folder used for the collection of test scripts/method if have.

## 3.6 testdesign folder building

This folder used for the collection of real test design.

The following description is based on FPGA(Diamond, ICECube2), other software may have different definition.

### 3.6.1 models folder building

“Models” folder used to place the models your design need, actually these files was generated by SCUBA engine,

Recommend setting:

a) If you only have one model file it is recommend using the name of “model\_top” to be both top module and file name.

### 3.6.2 others folder building

“others” folder used to place IP core files, NGO files and some other files.

Recommend setting:

NA

### 3.6.3 par folder building

“par” folder used to place the project files.

Recommend setting:

1. it’s better to name project file as prj\_top.ldf
2. it’s better to use default implement(impl1)

### 3.6.4 sim folder building

“sim” folder used to collect all simulation files:

Recommend setting:

1. The default test bench file name is “sim\_tb.v/vhd”
2. The default active-HDL macro file name is “ahdl.do”
3. The default ModelSIM macro file name is “msim.do”
4. The test vector input file name is “test\_vector.in” if you have.

#### 3. 6.4.1 TB file building

TB file will be used in simulation flow, it is recommend to run the following setting:

1. The default test bench file name is “sim\_tb.v/vhd”
2. The bench file top module name is “sim\_top”
3. Top RTL instance name is “UUT” (unit under test)

#### 3. 6.4.2 macro file building

Macro file (.do file) will be used to run simulation when script catches this file. Since a user was only required to supply a macro file for RTL simulation, to make it compatible with map/par simulation, the macro file should use the fixed format:

1. It is better to divide macro file into the different sections: configure, library map, source compile, test bench compile, preparing for simulation, simulation.
2. Every section will be surrounding by comments like “##<xx\_start/end>”, these comments or flags will be key pattern for script use, do not delete or modify.

##### 3.6.4.2.1 Ahdl macro file

Here is an example of active-HDL macro file:

-----------------------------------------------ahdl.do-------------------------------------------------------

#<START>

##<cfg\_start>

set IgnoreError 1

set dev\_lib $1

set pri\_lib $2

set gui\_cmd $3

##<cfg\_end>

##<lib\_start>

##<step1>construct a work lib

if $gui\_cmd = 'cmd'

vlib work

else

design create work .

design open work

adel -all

cd ../../

endif

##<step2>connect some other lib

vmap <lib\_name> $dev\_lib

##<lib\_end>

##compile source files if you use VHDL please use vcom

##<source\_start>

vlog ../source/ rtl\_source1.v/vhd

vlog ../models/model\_top.v/vhd

##<source\_end>

##<tb\_start>

vlog ./ sim\_source1.v/vhd

##<tb\_end>

##prepare for simulation

##<pre\_start>

radix -hex

##<pre\_end>

##start to run simulation

##<sim\_start>

vsim -novopt -lib work sim\_top -L <lib\_name>

if $gui\_cmd = 'cmd'

run 10us

quit

else

wave -noreg sim\_top/\*

run 10us

endif

##<sim\_end>

#<END>

-----------------------------------------------do end-------------------------------------------------------

Some requirement:

1. “rtl\_source1.v/vhd” should be the top source file, since the first RTL file in source compile section will be treated as top source file by script.
2. “sim\_source1.v/vhd” should be the top test bench file, since the first test bench file in test bench compile section will be treated as top test bench file by script.
3. We list three argument variables here: dev\_lib, pri\_lib, gui\_cmd by default, if you want to add some more libraries, please start from $4.
4. Please use a limited simulation time such as “10us” instead of “-all” which maybe entry an endless loop in command line simulation.
5. Lib\_name should be the real device simulation library, for example: if the dev\_lib is “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\ovi\_machxo3l\\ovi\_machxo3l.lib” the name for lib\_name is “ovi\_machxo3l”.

Some explanation:

1. Dev\_lib: device library which will be used in simulation, In active-HDL it’s an address like “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\ovi\_machxo3l\\ovi\_machxo3l.lib” while in ModelSIM it will be the location which you have compiled the device modules like ” D:\\BQS\_script\\test\_case\\Vlib\\ovi\_machxo3l”
2. Pri\_lib: first search library. Any library list here will be searched first when simulator encounter an unknown module. This library can be “work”, device library we list before or some another library such as PMI library address “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\pmi\_work\\pmi\_work.lib”
3. Gui\_cmd: the value for this variable should be “gui” or “cmd” which means run in GUI or command line. With this variable we can make this macro file compatible for GUI and command line.

Usages:

1. Run in GUI :
2. Open active-HDL simulation tool.
3. In the TCL window, use “pwd” and “cd” commands to change the current work path to your case path.
4. In the TCL window, type “do <do file name> <dev\_lib> [pri\_lib] [gui]”, variables in “<>” are must have while variables in “[]” can be omit.

If you not use “pri\_lib” in your macro file, it can be omit too and if we doesn’t find “pri\_lib” the default value “work” library will be use

1. Run in command line:
2. Locate your work path to your case path.
3. Type: vsimsa -l sim\_log.txt -do <do file name> <dev\_lib> <pri\_lib> <cmd>

##### 3.6.4.2.2 msim macro file

Here is an example of active-HDL macro file:

-----------------------------------------------msim.do-------------------------------------------------------

#<START>

##<cfg\_start>

set IgnoreError 1

set dev\_lib $1

set pri\_lib $2

set gui\_cmd $3

##<cfg\_end>

##get device simulation module

##<lib\_start>

##<step1>construct a work lib

vlib work

##<step2>connect some other lib

vmap <lib\_name>$dev\_lib

##<lib\_end>

##compile source files if you use VHDL please use vcom

##<source\_start>

vlog ../source/ rtl\_source1.v/vhd

vlog ../models/model\_top.v/vhd

##<source\_end>

##<tb\_start>

vlog ./sim\_source1.v/vhd

##<tb\_end>

##prepare for simulation

##<pre\_start>

radix -hex

##<pre\_end>

##start to run simulation

##<sim\_start>

vsim -novopt -lib work sim\_top -L <lib\_name>

if {$gui\_cmd == "cmd"} {

run 10us

quit

} else {

add wave \*

run 10us

}

##<sim\_end>

#<END>

-----------------------------------------------do end-------------------------------------------------------

Some requirement:

1. “rtl\_source1.v/vhd” should be the top source file, since the first RTL file in source compile section will be treated as top source file by script.
2. “sim\_source1.v/vhd” should be the top test bench file, since the first test bench file in test bench compile section will be treated as top test bench file by script.
3. We list three argument variables here: dev\_lib, pri\_lib, gui\_cmd by default, if you want to add some more libraries, please start from $4.
4. Please use a limited simulation time such as “10us” instead of “-all” which maybe entry an endless loop in command line simulation.
5. Lib\_name should be the real device simulation library, for example: if the dev\_lib is “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\ovi\_machxo3l\\ovi\_machxo3l.lib” the name for lib\_name is “ovi\_machxo3l”.

Some explanation:

1. Dev\_lib: device library which will be used in simulation, In active-HDL it’s an address like “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\ovi\_machxo3l\\ovi\_machxo3l.lib” while in ModelSIM it will be the location which you have compiled the device modules like ” D:\\BQS\_script\\test\_case\\Vlib\\ovi\_machxo3l”
2. Pri\_lib: first search library. Any library list here will be searched first when simulator encounter an unknown module. This library can be “work”, device library we list before or some another library such as PMI library address “C:\\lscc\\diamond\\3.1\\active-hdl\\Vlib\\pmi\_work\\pmi\_work.lib”
3. Gui\_cmd: the value for this variable should be “gui” or “cmd” which means run in GUI or command line. With this variable we can make this macro file compatible for GUI and command line.

Usages:

1. Run in GUI :
2. Open active-HDL simulation tool.
3. In the TCL window, use “pwd” and “cd” commands to change the current work path to your case path.
4. In the TCL window, type “do <do file name> <dev\_lib> [pri\_lib][ gui]”, variables in “<>” are must have while variables in “[]” can be omit.

If you do not need “pri\_lib” in your macro file, just leave it blank there, script will use “work” as default value.

1. Run in command line:
2. Locate your work path to your case path.
3. Type: vsim -l sim\_log.txt -c -do "do <do file name> <dev\_lib> <pri\_lib> <cmd>"

### 3.6.5 source folder building

“source” folder used to collect all RTL source files:

Recommend setting:

1. the top RTL file name is “rtl\_top”
2. the top module name is “rtl\_top”

## 3.9 Simulation lib building

Simulation lib is used to run simulation flow, since it can be used for the whole test suite (every case), so simulation lib folder will not be placed in test case folder and with different simulation tool we need configure a little different:

### 3.9.1 active-HDL lib building

Diamond have already build this library for us, you can location will based on the test diamond version: <diamond install path>/active-hdl/Vlib. You will find all device lib(both for Verilog and VHDL) are there.

### 3.9.2 ModelSIM lib building

We need build ModelSIM lib manually and place it in the test suite folder. The top lib name should be “Vlib” and the device or model lib name should use the name we find in active-HDL. For example:

#here is a simple structure for test suite

./BQS\_script test script

./test\_case1 test case

./Vlib simulation lib top folder for ModelSIM use

./ecp3 ecp3 VHDL lib for ModelSIM use

./ovi\_ecp3 ecp3 Verilog lib for ModelSIM use

./pmi\_work pmi\_work lib for ModelSIM use

…

./xxxx.bat some launch script CMD file

\*NOTE: Different ModelSIM version may have different library format for VHDL simulation. Please confirm it first.

### 3.9.3 LIB configure in info file

In every case there is an info file for simulation configuration if need. Since we build ModelSIM lib with the same name as active-HDL so the lib name are same, such as:

Dev\_lib = <ovi\_ecp3> don’t care the detail address for this lib

Pri\_lib =pmi\_work don’t care the detail address for this lib

\*Note: Script will search the device lib automatically, so you do not need to list the device library (ovi\_ecp3), we list the library here is for your understanding.

But for script it is different for different simulation tools:

For active-HDL:

Dev\_lib = ovi\_ecp3 EQUAL Dev\_lib = <diamond install path>/active-hdl/Vlib/ovi\_ecp3/ ovi\_ecp3.lib

Pri\_lib = pmi\_work EQUAL Pri\_lib = <diamond install path>/active-hdl/Vlib/pmi\_work/pmi\_work.lib

For ModelSIM

Dev\_lib = ovi\_ecp3 EQUAL Dev\_lib = <test suite path>/Vlib/ovi\_ecp3

Pri\_lib = pmi\_work EQUAL Pri\_lib = <test suite path>/Vlib/pmi\_work

# 4 Examples

## 4.1 Diamond case demo

<http://lshlabd0001/viewvc/platform/trunk/bqs_scripts/regression_suite/diamond_suite/>

## 4.2 icecube case demo

<http://lshlabd0001/viewvc/platform/trunk/bqs_scripts/regression_suite/icecube_suite/>